## 1.2.2 Number of Add on/certificate programs offered during 2023-2024

### INDEX



PRINCIPAL
M.I.E.T. ENGINEERING COLLEGE
GUNDUR, TIRUCHIRAPALLI - 620 007.

# M.I.E.T. ENGINEERING COLLEGE

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai)
UG - CSE, EEE & MECH Programs Accredited by NBA, New Delhi
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Trichy – Pudukkottai Road, Tiruchirappalli – 620 007. Phone:0431-2660 303
Website:www.miet.edu, E-mail:principalengg@miet.edu, contact@miet.edu


Date: 12.02.2024

To

The Principal

M.I.E.T Engineering College,

Trichy – 620007

Respected Sir,

Sub: Permission to conduct the value added course – Reg.

We have planned to conduct a value added course for our second and third year Electronics and Communication Engineering students from 12.02.2024 to 02.04.2024.

| Name of the Value Added Course | Course Coordinator |
|---|---|
| **Introduction to Verilog and VHDLprogramming** | **Mrs.P.Gayathri, AP/ECE** |

So kindly give us permission to conduct the course and to utilize the class room.

Thanking you

**Course Coordinator** **HoD/ECE** **Principal** 12/2/24.

[P. Gayathri]
AP/ECE

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12.02.2024

## CIRCULAR

**Sub:** Value added course

It is planned to conduct the value added course for the Second and Third Year Electronics and Communication Engineering students.

The Certificate Program is short term certificate courses which are designed and offered by our department for the benefit of our students. Certificate Program will be conducted at free of cost and based on the performance of the participated students, the merit certificate will be issued after the successful completion of the course.

Students those who are willing to attend the below mentioned course can enroll their name to the course coordinator.

| Name of the Value Added Course | Course Coordinator |
|---|---|
| **Introduction to Verilog and VHDL Programming** | **Mrs. P.Gayathri, AP/ECE** |
| **Commencement of course from 12.02.2024 to 17.04.2024** | |

Course Coordinator
[P Gayathri]
AP/ECE

IQAC Coordinator
[R. ANITHA]

HoD/ECE

Principal 12/2/24.

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**DEPARTMENT OF ECE**

**VALUE ADDED COURSE**

**Name of the course: Introduction to Verilog and VHDL Programming.**
**Course Code: EC12324**
**Course Coordinator: Mrs.P.Gayathri, AP/ECE**
**Total Hours: 45** **Academic Year: 2023-2024**

**COURSE OBJECTIVES:**

1. To know the basic language features of Verilog HDL and the role of HDL in digital logic design.
2. To know the behavioural modeling of combinational and simple sequential circuits.
3. To know the behavioral modeling of algorithmic state machines.
4. To know the synthesis of combinational and sequential descriptions.
5. To know the architectural features of programmable logic devices

**COURSE SYLLABUS:**

**Module 1** Introduction to Logic Design with Verilog : Structural models of combination logic, logic simulation, design verification, test methodology, propagation delay, truth table models of combinational and sequential logic with verilog modules, ports, gate types, gate delays, dataflow modelling, continuous assignments delays, expressions, operators, operands, operator types

**Module 2** Logic Design With Behavioral Models of Combinational And Sequential Logic : Behavioral modeling, data types for behavioral modeling, behavioral models of combinational logic, propagation delay and continuous assignments, lathes and level sensitive circuits in verilog, cyclic behavioural models of flip flops and latches, cyclic behavior and edge detection, a comparison of styles for behavioral modeling.

**Module 3** Behavioral models of multiplexers, encoders and decoders data flow model of a lfsr machines with multicycle operations, algorthmic state machine charts for behavioral modeling, asmd charts, behavioral models of counters, shift registers and register files, switch debounce, metastability, synchronizers for asynchronous signals.

**Module 4** Introduction to synthesis : synthesis of combinational logic, synthesis of sequential logic with latches, synthesis of three state devices and bus interfaces, synthesis of sequential logic with flip flops, synthesis of explicit state machines registered logic.

**Module 5** Programmable logic devices, storage devices, programmable logic array programmable array logic, programmability of PLDs CPLDs.

**Module-5 Mini project**

TOTAL PERIODS: 45

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**TEXT BOOK(s):**

1. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009. Detailed Syllabus(ECE) Page 105 of 201 R.V.R. & J.C.College of Engineering (Autonomous) R-16

2. Samir Palnitkar - Verilog HDL, 2nd edition, Pearson Education, 2003.

**Course Outcome:**

The students will be able to:

**CO1**. Demonstate knowledge on HDL design flow,digital circuits design ,switch de-bouncing, metastability, memory devices applications .

**CO2**. Design and develop the combinational and sequential circuits using behavioral modeling.

**CO3**. Solving algorithmic state machines using hardware description language.

**CO4**. Analyze the process of synthesizing the combinational and sequential descriptions.

**CO5**. Memorizing the advantages of programmable logic devices and their description in Verilog.

**Course instructor** **HoD/ECE** **Principal**

[P. Gayathri]
AP/ECE

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## Department Of Electronics And Communication Engineering

### Willing Student List

**Name Of The Course: Introduction To Verilog And VHDL Programming.**
**Course Code : EC12324**
**Coordinator: Mrs.P.Gayathri AP/ECE**
**Academic Year: 2023-2024**

| S.No | Register No. | Name Of The Student | Verilog & VHDL |
|---|---|---|---|
| 1. | E1224001 | AARTHI A | ✓ |
| 2. | E1224002 | ABDUL AJISH N | ✓ |
| 3. | E1224003 | AGALYA D | ✓ |
| 4. | E1224004 | ATCHAYA T | ✓ |
| 5. | E1224005 | AYYAPPAN G | ✓ |
| 6. | E1224006 | CALEP JABEZ.M | ✓ |
| 7. | E1224007 | CHANDRU M G | ✓ |
| 8. | E1224008 | DHARANI R | ✓ |
| 9. | E1224009 | FAAHIM M | ✓ |
| 10. | E1224010 | GOPINATH N | ✓ |
| 11. | E1224011 | GURUMOORTHI K | ✓ |
| 12. | E1224012 | HARI PRASATH P | ✓ |
| 13. | E1224013 | HARISH MOHAMMED A | ✓ |
| 14. | E1224014 | HARISH T | ✓ |
| 15. | E1224015 | JEEVA T | ✓ |
| 16. | E1224016 | KAILASA MANICKAM.M | ✓ |
| 17. | E1224017 | KARTHIKEYAN.S | ✓ |
| 18. | E1224018 | KEERTHI VARSHAN P B | ✓ |
| 19. | E1224019 | KISHORE KUMAR R | ✓ |
| 20. | E1224020 | KISHORE N | ✓ |

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| | | | |
|---|---|---|---|
| 21. | E1224021 | LOGESWARAN A | |
| 22. | E1224022 | MAHESWARAN T | |
| 23. | E1224023 | MANUSHA S | |
| 24. | E1224024 | MOHAMED ABDULLAH K | |
| 25. | E1224025 | MOHAMED ASWITH A | |
| 26. | E1224026 | MOHAMED HAMTHAN A | |
| 27. | E1224027 | MOHAMED SHAJID.N | |
| 28. | E1224028 | MOHAMMED SHARIF S | |
| 29. | E1224029 | NASRIN A | |
| 30. | E1224030 | PARTHIBAN S | |
| 31. | E1224031 | RAGAVAN G | |
| 32. | E1224032 | RAHEEM M | |
| 33. | E1224033 | RIZA AHAMED J | |
| 34. | E1224034 | ROYAL VIGNESHWAR E S | |
| 35. | E1224036 | SEMMOZHIVARMAN P | |
| 36. | E1224037 | SIVAMANICKAM M | |
| 37. | E1224038 | SYED BARVEES J | |
| 38. | E1224039 | SYED HUSSAIN S | |
| 39. | E1224040 | VAAZIM AHAMED A | |
| 40. | E1224041 | VENKADESH PRASATH S | |
| 41. | E1224042 | VERGIN FRANKIYA K | |
| 42. | E1224043 | VIGNESH KUMAR L | |
| 43. | E1224044 | YAHYA B | |
| 44. | E1224045 | YOGESWARI S | |
| 45. | E2224046 | ANDREW XAVIER J | |
| 46. | E2224047 | MOHAMED AJMAL M | |
| 47. | E2224048 | MOULESWARI M | |
| 48. | E2224049 | PRAKASH KUMAR S | |
| 49. | E2224050 | SAHUL HAMEED M | |

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| | | | |
|---|---|---|---|
| 50. | 812421106001 | Ahamed Yaseen S | |
| 51. | 812421106002 | Alageshwari M | |
| 52. | 812421106003 | Ameen Mohideen S | |
| 53. | 812421106005 | Asraf Ali A | |
| 54. | 812421106006 | Baby Shalini R | |
| 55. | 812421106007 | Fahadhu Rilwan A | |
| 56. | 812421106008 | Farzana Begum M | |
| 57. | 812421106010 | Jayakumar E | |
| 58. | 812421106012 | Madhumitha M | |
| 59. | 812421106013 | Mohamed Amjath S | |
| 60. | 812421106014 | Mohamed Kaja Bhasith K S | |
| 61. | 812421106016 | Mohamed Naufal J | |
| 62. | 812421106017 | Mohamed Suhaj B | |
| 63. | 812421106018 | Mohamed Tharik A | |
| 64. | 812421106019 | Mohamed Vasim Hussain K | |
| 65. | 812421106021 | Naveen Kumar N | |
| 66. | 812421106022 | Pragadeeswaran V | |
| 67. | 812421106023 | Sanjay V | |
| 68. | 812421106026 | Sriganth S | |
| 69. | 812421106028 | Sujith Munna S | |
| 70. | 812421106029 | Syed Ashik S | |
| 71. | 812421106030 | Vimal R | |
| 72. | 812421106031 | Vishnu Varthan S | |
| 73. | 812421106301 | Aadithiya K | |
| 74. | 812421106303 | Dalvin Gnana Raja D | |
| 75. | 812421106304 | Deva S | |
| 76. | 812421106305 | Harish V | |
| 77. | 812421106306 | Maheswari G | |
| 78. | 812421106307 | Manjari R | |
| 79. | 812421106308 | Marimuthu A | |
| 80. | 812421106309 | Shaik Bareeth M | |

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| | | | |
|---|---|---|---|
| 81. | 812421106310 | Shanmuganathan S | ✓ |
| 82. | 812421106311 | Thowfiqueahamed H | ✓ |
| 83. | 812421106312 | Vijay K | ✓ |

**Course Coordinator**

[P. Gayathri]
AP/ECE

**HOD/ECE**

**Principal**

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## DEPARTMENT OF BIOMEDICAL ENGINEERING

Value Added Course (II Year – IV Semester)

**Course Delivery**

**Name of the Course: Introduction To Verilog and VHDL Programming**
**Course Code:EC12324**

**Course Coordinator: P.Gayathri, AP/ECE**

**Total Hours: 30**
**Academic Year: 2023-2024**

| Sl.No | Topics to be Covered | Hours | Date of Deliver |
|---|---|---|---|
| 1. | MOS Structure | 1 | 12.02.2024 |
| 2. | NMOS | 2 | 14.02.2024 |
| 3. | PMOS and CMOS fabrication | 3 | 16.02.2024 |
| 4. | Depletion Transistor. | 4 | 16.02.2024 |
| 5. | MOS device design equations: drain current-voltage | 5 | 16.02.2024 |
| 6. | threshold voltage, transconductance. NMOS Inverter and Transfe characteristics | 6 | 17.02.2024 |
| 7. | pull up and pull down ratios of NMOS | 7 | 19.02.2024 |
| 8. | alternative forms of pull up | 8 | 21.02.2024 |
| 9. | CMOS Inverter and transfer characteristics | 9 | 22.02.2024 |
| 10. | Latch-up in CMOS circuits | 10 | 23.02.2024 |
| 11. | Scaling Models, Scaling factors for device parameters, | 11 | 24.02.2024 |
| 12. | Limitations of Scaling. | 12 | 06.03.2024 |
| 13. | Introduction to VLSI design cycle | 13 | 07.03.2024 |
| 14. | Computer-aided design tools for digital systems | 14 | 08.03.2024 |
| 15. | Hardware description language: | 15 | 09.03.2024 |
| 16. | VHDL, features, Data objects, Classes and data types, | 16 | 10.03.2024 |
| 17. | Operators, Subprograms, Overloading. | 17 | 11.03.2024 |

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| Sl.No | Topics to be Covered | Hours | Date of Deliver |
|---|---|---|---|
| 18. | Behavioral, structural, data flow style of modeling | 18 | 12.03.2024 |
| 19. | Assignment statements, Sequential Statements and Proces Conditional Statements | 19 | 21.03.2024 |
| 20. | Case Statements, Loops, Resolution Functions, Packages Libraries, Concurrent Statements. | 20 | 23.03.2024 |
| 21. | Packages & Libraries, Concurrent Statements. | 21 | 29.03.2024 |
| 22. | Combinational Circuit Design such as such as Multiplexer Encoders, Decoders | 22 | 6.04.2024 |
| 23. | Code Converters, Comparators, | 23 | 14.04.2024 |
| 24. | Implementation of Boolean functions etc., Sequential Circu Design such as Shift registers | 24 | 21.04.2024 |
| 25. | Counters, Flip-flops | 25 | 22.04.2024 |
| 26. | Mini Project | 26 | 27.04.2024 |
| | | 27 | 02.05.2024 |
| | | 28 | 03.05.2024 |
| | | 29 | 23.05.2024 |
| | | 30 | 23.05.2024 |

**Course Coordinator** **HoD/ECE** **Principal**

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## Resource Person Details

| | |
|---|---|
| **Title of the program** | **Introduction to verilog and VHDL Programming** |
| **Course Code** | **EC23241** |
| **Duration and timing of the program** | **30 Hrs, 04.45 pm to 06.15 pm** |
| **Name of the resource person** | **Mrs.P.Gayathri, AP/ECE** |
| **Photo of the resource person** |  |
| **Email address** | Gayu.nov29@gmail.com |
| **Contact number** | 9385579072 |
| **Designation** | Assistant Professor |
| **Educational qualification** | ➢ Completed B.E., JCET,Trichy<br>➢ Completed M.E.,Prist University,Tanjavur |
| **Experience** | ➢ Teaching Experience – 10 year |

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

Value Added Courses (III Year – VI Semester)

**Attendance Sheet**

Name of the course: **Introduction to verilog and VHDL Programming.**
Course code: EC12324
Course coordinator: Mrs. P.Gayathri, AP/ECE
Academic Year: 2023-24

| SL.NO | ROLL NO | STUDENT NAME | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 12/2/24 | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | ✓ | | ✓ |
| 1 | 812421106001 | AHAMED YASEEN.S | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | | ✓ |
| 2 | 812421106002 | ALAGESWARI.M | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | ✓ |
| 3 | 812421106003 | AMEEM MOHIDEEN.S | ✓ | ✓ | ✓ | | ✓ | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | |
| 4 | 812421106006 | ASARAB ALI .A | ✓ | | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ |
| 5 | 812420106007 | BABY SHALINI .R | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 6 | 812420106008 | FAHADNU RILWAN .A | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ |
| 7 | 812420106009 | FARZANA BEGUM .M | ✓ | ✓ | | ✓ | ✓ | ✓ | | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 8 | 812420106010 | JAYAKUMAR .E | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | | ✓ |
| 9 | 812420106012 | MADHUMIDHA. M | ✓ | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | |
| 10 | 812421106013 | MOHAMED AMJATH .S | ✓ | ✓ | | ✓ | | ✓ | ✓ | | ✓ | | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ |
| 11 | 812421106014 | MOHAMED KAJA BHASTH .K.S | ✓ | ✓ | | ✓ | | ✓ | | | ✓ | | ✓ | ✓ | | ✓ | | | ✓ | ✓ | ✓ | ✓ |

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| SL.NO | ROLL NO | STUDENT NAME | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 | 812420106316 | MOHAMED NAUFAL .J | | | | | | | | | | | | | | | | | | | | |
| 13 | 812420106317 | MOHAMED SUHAJ .B | | | | | | | | | | | | | | | | | | | | |
| 14 | 812420106318 | MOHAMED THARK .A | | | | | | | | | | | | | | | | | | | | |
| 15 | 812420106319 | MOHAMED VASIM HUSSAIN .K | | | | | | | | | | | | | | | | | | | | |
| 16 | 812420106321 | NAVEEN KUMAR.N | | | | | | | | | | | | | | | | | | | | |
| 17 | 812420106322 | PRAGADEESWARAN .V | | | | | | | | | | | | | | | | | | | | |
| 18 | 812420106023 | SANJAY .V | | | | | | | | | | | | | | | | | | | | |
| 19 | 812421106026 | SRIGANTH .S | | | | | | | | | | | | | | | | | | | | |
| 20 | 812420106028 | SUJITH MUNNA.S | | | | | | | | | | | | | | | | | | | | |
| 21 | 812420106029 | SYED ASHIK .S | | | | | | | | | | | | | | | | | | | | |
| 22 | 812420106030 | VIMAL .R | | | | | | | | | | | | | | | | | | | | |
| 23 | 812420106031 | VISHNU VARTHAN .S | | | | | | | | | | | | | | | | | | | | |
| 24 | 812421106301 | AADITHIYA .K | | | | | | | | | | | | | | | | | | | | |
| 25 | 812421106303 | DALVIN GAANA RAJA.D | | | | | | | | | | | | | | | | | | | | |
| 26 | 812421106304 | DEVA .S | | | | | | | | | | | | | | | | | | | | |
| 27 | 812421106305 | HARISH.V | | | | | | | | | | | | | | | | | | | | |
| 28 | 812421106306 | MAHESWARI.G | | | | | | | | | | | | | | | | | | | | |
| 29 | 812421106307 | MANJARI .R | | | | | | | | | | | | | | | | | | | | |

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| SL.NO | ROLL NO | STUDENT NAME | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 12/2/24 | | | | | | | | | | | | | | | | | | | |
| 30 | 812421106308 | MARIMUTHU.A | | | | | | | | | | | | | | | | | | | | |
| 31 | 812421106309 | SHAIK BAREETH.M | | | | | | | | | | | | | | | | | | | | |
| 32 | 812421106310 | SHANMUGA NATHAN .S | | | | | | | | | | | | | | | | | | | | |
| 33 | 812421106311 | THOWFIQUE AHAMED .H | | | | | | | | | | | | | | | | | | | | |
| 34 | 812421106312 | VIJAY .K | | | | | | | | | | | | | | | | | | | | |
| Total No. of students Present | | | 20 | 28 | 27 | 28 | 30 | 20 | 25 | 27 | 30 | 29 | 28 | 31 | 30 | 32 | 30 | 29 | 30 | 29 | 28 | 27 |
| Total No. of students Absent | | | 14 | 6 | 7 | 5 | 3 | 14 | 10 | 7 | 5 | 5 | 7 | 4 | 3 | 2 | 4 | 5 | 4 | 5 | 7 | 7 |
| Signature of Course Coordinator | | | | | | | | | | | | | | | | | | | | | | |

**Course Coordinator** **HOD/ECE** **Principal**

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Website:www.miet.edu, E-mail:principalengg@miet.edu, contact@miet.edu

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

Value Added Courses (III Year – VI Semester)

**Attendance Sheet**

**Name of the course: Introduction to verilog and VHDL Programming.**
**Course code: EC12324**
**Course coordinator: Mrs. P.Gayathri, AP/ECE**
**Academic Year: 2023-24**

| SL.NO | ROLL NO | STUDENT NAME | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Att | | | | | | | | | |
| 1 | 812421106001 | AHAMED YASEEN.S | a | / | / | / | / | a | / | / | / | / |
| 2 | 812421106002 | ALAGESWARI.M | / | / | / | a | / | / | / | a | / | a |
| 3 | 812421106003 | AMEEM MOHIDEEN.S | / | / | / | / | / | / | / | / | / | / |
| 4 | 812421106006 | ASARAB ALI .A | / | / | / | / | a | / | / | / | / | / |
| 5 | 812420106007 | BABY SHALINI .R | / | a | / | / | / | / | / | / | / | / |
| 6 | 812420106008 | FAHADNU RILWAN .A | / | / | / | / | / | / | a | / | / | / |
| 7 | 812420106009 | FARZANA BEGUM .M | / | / | / | / | / | / | / | / | / | / |
| 8 | 812420106010 | JAYAKUMAR .E | / | / | / | / | / | / | / | a | / | a |
| 9 | 812420106012 | MADHUMIDHA. M | a | / | / | a | / | / | / | / | / | / |
| 10 | 812421106013 | MOHAMED AMJATH .S | / | / | / | / | / | / | a | / | / | / |
| 11 | 812421106014 | MOHAMED KAJA BHASTH .K.S | / | a | / | / | / | / | / | / | a | / |

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| SL.NO | ROLL NO | STUDENT NAME | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 | 812420106316 | MOHAMED NAUFAL .J | | | | | | | | | | |
| 13 | 812420106317 | MOHAMED SUHAJ .B | | | | | | | | | | |
| 14 | 812420106318 | MOHAMED THARK .A | | | | | | | | | | |
| 15 | 812420106319 | MOHAMED VASIM HUSSAIN .K | | | | | | | | | | |
| 16 | 812420106321 | NAVEEN KUMAR.N | | | | | | | | | | |
| 17 | 812420106322 | PRAGADEESWARAN .V | | | | | | | | | | |
| 18 | 812420106023 | SANJAY .V | | | | | | | | | | |
| 19 | 812421106026 | SRIGANTH .S | | | | | | | | | | |
| 20 | 812420106028 | SUJITH MUNNA.S | | | | | | | | | | |
| 21 | 812420106029 | SYED ASHIK .S | | | | | | | | | | |
| 22 | 812420106030 | VIMAL .R | | | | | | | | | | |
| 23 | 812420106031 | VISHNU VARTHAN .S | | | | | | | | | | |
| 24 | 812421106301 | AADITHIYA .K | | | | | | | | | | |
| 25 | 812421106303 | DALVIN GAANA RAJA.D | | | | | | | | | | |
| 26 | 812421106304 | DEVA .S | | | | | | | | | | |
| 27 | 812421106305 | HARISH.V | | | | | | | | | | |
| 28 | 812421106306 | MAHESWARI.G | | | | | | | | | | |
| 29 | 812421106307 | MANJARI .R | | | | | | | | | | |

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| SL.NO | ROLL NO | STUDENT NAME | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 30 | 812421106308 | MARIMUTHU.A | / | a | / | / | a | / | / | / | / | a |
| 31 | 812421106309 | SHAIK BAREETH.M | / | / | / | / | / | / | / | a | / | / |
| 32 | 812421106310 | SHANMUGA NATHAN .S | a | / | / | a | / | / | / | / | / | / |
| 33 | 812421106311 | THOWFIQUE AHAMED .H | / | / | a | / | / | / | / | / | / | / |
| 34 | 812421106312 | VIJAY .K | / | / | / | / | / | a | / | / | / | a |
| Total No. of students Present | | | 30 | 28 | 29 | 25 | 24 | 27 | 30 | 26 | 31 | 26 |
| Total No. of students Absent | | | 3 | 6 | 7 | 9 | 6 | 7 | 4 | 8 | 3 | 8 |
| Signature of Course Coordinator | | | N | N | N | N | N | N | N | N | N | N |

**Course Coordinator** **HOD/ECE** **Principal**

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## Report

**Name of the course: Introduction to verilog and VHDL Programming**
**Course Code: EC23241**
**Course Coordinator: Mrs.P.Gayathri, AP/ECE**

**Total Hours: 30** **Academic Year: 2023-2024**

I hereby affirm that the entire course contents listed in the course syllabus of the certificate program **"Introduction to verilog and VHDL Programming"** have educated to the students as the part of the prescribed co – curricular activities through Certificate Program.

They have been given hands on session on the topics mentioned and students clearly understood the hardware configuration of the system.

The certificate program titled as **"Introduction to verilog and VHDL Programming"** has been conducted in the beginning of the semester and course delivery along with attendance of the students was recorded.

All the students were actively attended this certificate Program and performed well throughout the program and eligible students received the certificate.

**Course Coordinator** **HoD/ECE** **Principal**

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## Questions and Answers

1.

Which among the following is a process of transforming RTL to a gate-level netlist?

- A. Simulation
- B. Optimization
- C. Synthesis
- D. Verification

Correct Answer
C. Synthesis

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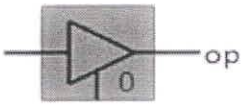
2.




The output of the following logic =?

- A. Logic 0
- B. Logic 1
- C. X
- D. Z

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Correct Answer
D. Z

.

Rate this question:

- 3.

#40 $finish indicates

A. End of simulation time

B. End of simulation at 40-time units

C. Suspend simulation at 40-time units

D. None

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Correct Answer
A. End of simulation time

Rate this question:
2
1

- 4.

The characteristic equation of 'T' Flip flop is given by

- A. $Q(n+1) = T\,Q+T'Q'$
- B. $Q(n+1) = T+ Q'T'$
- C. T
- D. None

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Correct Answer
D. None

- 5.

The hexadecimal number 'A0' has the decimal value equivalent to:

- A. 80
- B. 256
- C. 100
- D. 160

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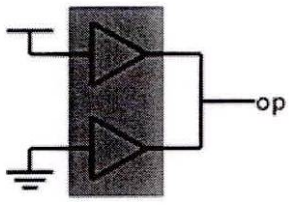
Correct Answer
D. 160

6.




The output of the following logic =?

- A. Logic 0
- B. Logic 1
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C

D.

Z

Correct Answer
C. X

7.

$(734)_8 = (\ )_{16}$

C

A.

C1D

C

B.

DC1

C

C.

1CD

C

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D.

1DC

Correct Answer
D. 1DC

8.

The full form of VLSI is _____.

A.

Very Long Single Integration

B.

Very Least Scale Integration

C.

Very Large Scale Integration

D.

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Very Long Scale Integration

Correct Answer
C. Very Large Scale Integration

.

**Rate this question:**

- 9.

VHDL stands for

- A. Very High-Speed Integrated Circuit Hardware Description Language
- B. Very High Description Langauge
- C. Verilog Hardware Description Language

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D.

None

Correct Answer
A. Very High-Speed Integrated Circuit Hardware Description Language

.

**Rate this question:**
1
0

- 10.

The digital logic family which has minimum power dissipation is:

- A. TTL
- B. RTL
- C. DTL

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D.

CMOS

Correct Answer
D. CMOS

**Rate this question:**

11.

ASIC stands for:

A.

Application speedy integrated circuit

B.

Application-specific integrated circuit

C.

Advanced speed integrated circuit

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D.

Advanced standard integrated circuit

Correct Answer
B. Application-specific integrated circuit

**Rate this question:**
2
0

- 12.

A 2-input XOR gate can be worked as an Inverter (NOT Gate) if a =? & b =?

○

A.

A = a , b =0

○

B.

A = a , b =1

○

C.

A = b , b= a

○

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D.

None

Correct Answer
B. A = a , b =1

**Rate this question:**

- 13.

Which model uses transistors as their basic components?

A.

Switch level

B.

Gate Level

C.

Circuit Level

D.

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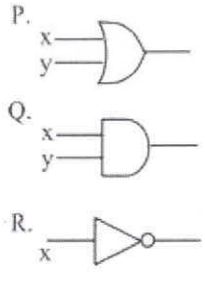
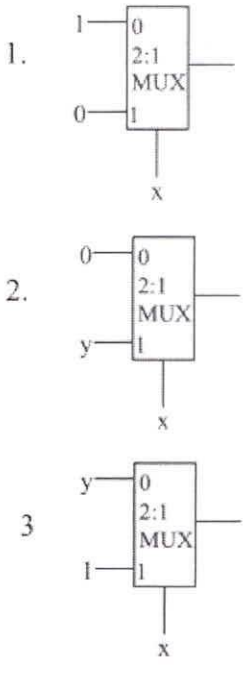
Layout Level

Correct Answer
A. Switch level

Rate this question:
1
0

- 14.




Match the following:

C

A.

P – 3 Q – 2 R – 1

C

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B.

P – 3 Q–1 R – 2

C.

C.

P – 2 Q –3 R –1

C

D.

None

Correct Answer
A. P – 3 Q – 2 R – 1

15.

What is the default value of the reg data type?

C

A.

0

C

B.

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1

C.

Z

D.

X

Correct Answer
D. X

Rate this question:

16.

The Gray code for decimal number 6 is equivalent to:

A.

1100

B.

1001

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C

C.

0101

C

D.

0110

Correct Answer
C. 0101

**Rate this question:**
1
0

17.

The Boolean expression (A'B+AB'+AB) is equivalent to:

C

A.

A+B

C

B.

A'+B

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C.

(A+B)'

D.

A.B

Correct Answer
A. A+B

Rate this question:

18.

What is the time period of clock #20 clock = ~clock?

A.

10

B.

20

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C.

40

C

D.

50

Correct Answer
C. 40

Rate this question:

19.

Verilog is case sensitive.

C

A.

True

C

B.

False

Correct Answer
A. True

Rate this question:
1

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0

20.

The FPGA is abbreviated as:

A.

First programmable Gate Array

B.

Field Programmable Gate Array

C.

Field Post Gate Array

D.

Field Program Gate Array

Correct Answer
B. Field Programmable Gate Array

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## COURSE COMPLETION CERTIFICATE

This certificate is awarded to Mr/Ms AHAMED YASEEN.S of **MIET Engineering College** has completed the value added course on **Introduction to verilog and VHDL Programming** organized by Department of Electronics and Communication Engineering during the Academic year 2023-2024 from 12.02.24 to 17.04.2024.

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Course Coordinator HOD Principal